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09/301,853	04/29/1999	KAZUHISA OHBUCHI	FUJS-16.073	6159

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EXAMINER

LAMARRE, GUY J

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/301,853

Applicant(s)

OHBUCHI ET AL.

Examiner

Guy J. Lamarre, P.E.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-53 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-53 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 April 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

Response to Amendment

0. This office action is in response to Applicants' **Amendment**, filed on 23 January 2002.

0.1 Claims 1-4, 7, 10-11, 14 and 17-18 are amended, Claims 19-53 are added. Claims 1-53 remain pending.

0.2 The rejections of record to Claims 1-18 stand withdrawn in response to Applicants' **Amendment**, filed on 23 January 2002.

0.3 The objections of record to the drawings and the specification stand maintained in response to Applicants' **Amendment**, filed on 23 January 2002.

0.4 Claims 1-53 are now rejected under 35 U.S.C. 103(a) as being unpatentable as follows.

Response to Arguments

1. Applicants' arguments, filed 23 January 2002, have been fully considered, and are deemed persuasive only to the extent that the approach, whereby random rearrangement of data is effected by exchanging data units at least between rows and columns, is not specifically disclosed by the prior art of record. However such data rearrangement means is well known and is clearly disclosed in Fig. 1 by **de Almeida et al.**, e.g., a 25-bit data is represented or controllably stored in matrix form or array, b1..b25 (left matrix), and said 25-bit data is randomly rearranged or de-spread or spread by exchanging data bits or units between columns and rows (right matrix). Said randomly rearranged 25-bit data is subsequently transferred or transmitted via a medium, recovered at a receiving station and undergoes a reverse permutation process. **de Almeida et al.** shows that such random data manipulation optimizes burst error correction processing.

Claim Rejections - 35 USC ' 103

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

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claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2.1 **Claims 1-53** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Lin et al.** (US Patent No. 5,068,878; February 6, 1990) in further view of **de Almeida et al.** (Two-Dimensional Interleaving Using the Set Partitioning Technique; IEEE, Aug. 1994).

As per Claims 1, 2, 3, 10, 17-24, 31-32, 35-36, 43, 46 and 49, Admitted prior art substantially discloses the procedure for the claimed interleaving method comprising the steps of: arranging data to be transmitted in a matrix; and randomly rearranging or spreading at least either columns or rows of said data and outputting said rearranged data in time series. {See **Admitted prior art**, Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted or spread row or column-wise in a random fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving or de-spreading) to recover said data; and control means to perform data shuffling and re-ordering; means to perform error detection and correction (page 3 line 25); means for data communication or transmission via radio or antenna means (page 1 line 17).} **Not specifically described** in detail in **Admitted prior art** is the step whereby random rearranging by either columns or rows of data is performed in time series or sequentially.

However such approach is well known. For example, **Lin et al.**, in an analogous art, discloses algorithms wherein such techniques are described. {See **Lin et al.**, Id., Abstract.}

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Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of the **Admitted prior art** by including therein a mathematical method as taught by **Lin et al.**, because such modification would provide the procedure disclosed in the **Admitted prior art** with a technique whereby the “[*The*] controller 100 then allows the flow of data from the data source 101 to continue. Referring to FIG. 3, it will be appreciated that the resynchronization signals 134, 136, 138, 140, 154 are thereby recordable on the tape 77 in a pseudo-random fashion relative to the interleave block boundaries. It will be noted that the resynchronization signals 134-154 are inserted in addition to the recorded data bytes; the flow of data being momentarily interrupted to accommodate the recording of the resynchronization signals.” {See **Lin et al.**, col. 7 line 17-et seq.}

While the **Admitted prior art** and **Lin et al** substantially disclose the procedure for the claimed invention, **they fail to specifically describe** in detail the concept whereby random rearrangement of data is effected by exchanging data units at least between rows and columns.

However, such technique is well known in data processing systems, e.g., **de Almeida et al.**, in an analogous art, discloses an algorithm wherein such random rearrangement means is depicted. {See **de Almeida et al.**, Id., Example 1, Fig.1 and Table 1.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Admitted prior art** and **Lin et al** by including therein the technique as disclosed by **de Almeida et al.** because such modification would provide the procedure of **Admitted prior art** and **Lin et al** with a method whereby “*simple random-error-correcting codes can be used to correct clusters of errors, instead of the more complex burst-error-correcting codes.*” {See **de Almeida et al. Id.**, SUMMARY: para. 1 last sentence, and col. 1 penultimate para.}

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As per Claims 4, 11, 25-26, 44-45, 47-48, 50-53, Lin et al. discloses the procedure for the claimed interleaving apparatus according to claim 3(10), wherein said first control unit comprises a first write controlling unit for generating a write address to be used to write said data to be transmitted in said first storing unit with said data to be transmitted arranged in a matrix and at least either columns or rows of said data to be transmitted randomly rearranged and for writing said data to be transmitted in said first storing unit, and said first control unit reads said data to be transmitted stored in said first storing unit in the order of addresses. {See Lin et al., col. 5 line 67-et seq., for data writing means effected by “*controller 100 which now sequences the changeover so that RAM 96 is read out and the RAM 96' is written into, as previously mentioned (FIG. 4).*” }

As per Claims 5, 12, 27-30, Lin et al. discloses the procedure for the claimed interleaving apparatus according to claim 4(11), wherein said first write control unit comprises a column number generating unit for randomly generating column numbers and a row number generating unit for randomly generating row numbers, and said first write control unit writes said data to be transmitted in said first storing unit with numbers generated by said column number generating unit and said row number generating unit as said write address to write said data to be transmitted in said first storing unit.. {See Lin et al., col. 5 line 67-et seq., for data writing means effected by “*controller 100 which now sequences the changeover so that RAM 96 is read out and the RAM 96' is written into, as previously mentioned (FIG. 4).*” } Also refer to **Admitted prior art**, Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a random fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering

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(de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.}

As per Claims 6, 13, 39-42, Lin et al. discloses the procedure for the claimed interleaving apparatus according to claim 5(12), 2 wherein each of said column number generating unit and said row number generating unit is configured with a memory for holding numbers used as addresses in a predetermined order {See Lin et al. col. 6 lines 17- et seq., wherein for address generation means via counter 108.}

As per Claims 7, 14, 33-34, Lin et al. discloses the procedure for the claimed interleaving apparatus according to claim 3(10), wherein said first control unit writes said data to be transmitted in said first storing unit in the order of addresses, and said first control unit comprises a first read controlling unit for generating a read address to be used to read said data to be transmitted from said first storing unit with said data to be transmitted stored in said first storing unit arranged in a matrix and at least either columns or rows of said data to be transmitted randomly rearranged to read said data to be transmitted. {See Lin et al., col. 5 line 67-et seq., for data writing means effected by “*controller 100 which now sequences the changeover so that RAM 96 is read out and the RAM 96' is written into, as previously mentioned (FIG. 4).* } Also refer to **Admitted prior art**, Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a random fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.}

As per Claims 8, 15, 37-38, Lin et al. discloses the procedure for the claimed interleaving apparatus according to claim 7 (14), wherein said first read control unit comprises a

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column number generating unit for randomly generating column numbers and a row number generating unit for randomly generating row numbers, and said first read control unit reads said data to be transmitted from said first storing unit with numbers generated by said column number generating unit and said row number generating unit as said read address. {See **Lin et al.**, col. 5 line 67-et seq., for data writing means effected by "*controller 100 which now sequences the changeover so that RAM 96 is read out and the RAM 96' is written into, as previously mentioned (FIG. 4).* } Also refer to **Admitted prior art**, Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a random fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering. }

As per **Claims 9, 16, Lin et al.** discloses the procedure for the claimed The interleaving apparatus according to claim 8(15), wherein each of said column number generating unit and said row number generating unit is configured with a memory for holding numbers used as addresses in a predetermined order {See **Lin et al.**, col. 7 lines 35- et seq., wherein predetermined order means is provided for permuting information. }

2.2 Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Azuma et al.** (US Patent No. 4959863; June 2, 1988) in further view of **de Almeida et al.** (Two-Dimensional Interleaving Using the Set Partitioning Technique; IEEE, Aug. 1994).

As per **Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49, Admitted prior art** substantially discloses the procedure for the claimed interleaving method comprising the steps of: arranging data to be transmitted in a matrix; and randomly rearranging at least either columns or rows of said data and outputting said rearranged data in time series. {See **Admitted**

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prior art, Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a random fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.} **Not specifically described** in detail in **Admitted prior art** is the step whereby random rearranging by either columns or rows of data is performed in time series or sequentially.

However such approach is well known. For example, **Azuma et al.**, in an analogous art, discloses algorithms wherein such techniques are described. {See **Azuma et al.**, Id., Abstract.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of the **Admitted prior art** by including therein a mathematical method as taught by **Azuma et al.**, because such modification would provide the procedure disclosed in the **Admitted prior art** with a technique whereby the “[*The*] *decimated signal sequence (signal vector) $Y_{sup.i}$ ($Z_{sup.16}$) is permuted by a multiplication by the permutation matrix $[T]$ of 8.times.8. In this case, the row element of the permutation matrix is 0 or 1 (the sum being 1), and element of this matrix is 0 or 1 (the sum being 1). The permutation matrix is a fixed permutation if constant with time, and a variable permutation if variable. In the scramble processing, the rows of this matrix are permuted at random, and the number of combinations is usually $n!$ for an n .times. n matrix.” {See **Azuma et al.**, col. 10 line 59-et seq.}*

While the **Admitted prior art** and **Azuma et al** substantially disclose the procedure for the claimed invention, **they fail to specifically describe** in detail the concept whereby random rearrangement of data is effected by exchanging data units at least between rows and columns.

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However, such technique is well known in data processing systems, e.g., **de Almeida et al.**, in an analogous art, discloses an algorithm wherein such random rearrangement means is depicted. {See **de Almeida et al.**, Id., Example 1, Fig.1 and Table 1.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Admitted prior art** and **Azuma et al** by including therein the technique as disclosed by **de Almeida et al.** because such modification would provide the procedure of **Admitted prior art** and **Azuma et al** with a method whereby "*simple random-error-correcting codes can be used to correct clusters of errors, instead of the more complex burst-error-correcting codes.*" {See **de Almeida et al. Id.**, SUMMARY: para. 1 last sentence, and col. 1 penultimate para.}

2.3 Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Yamaguchi et al.** ("Turbo Code", a new coding system approaching theoretical Shannon limits, is born in France; NIKKEI ELECTRONICS, July 13, 1988) in further view of **de Almeida et al.** (Two-Dimensional Interleaving Using the Set Partitioning Technique; IEEE, Aug. 1994).

As per Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49, Admitted prior art substantially discloses the procedure for the claimed interleaving method comprising the steps of: arranging data to be transmitted in a matrix; and randomly rearranging at least either columns or rows of said data and outputting said rearranged data in time series. {See **Admitted prior art**, Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a random fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.} **Not specifically described** in detail in **Admitted prior art** is the step whereby

random rearranging by either columns or rows of data is performed in time series or sequentially.

However such approach is well known. For example, **Yamaguchi et al.**, in an analogous art, discloses algorithms wherein such techniques are described. {See **Yamaguchi et al.**, Id., Excerpt translation : page 1 first and second paras. last line.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of the **Admitted prior art** by including therein a random permutation method as taught by **Yamaguchi et al.**, because such modification would provide the procedure disclosed in the **Admitted prior art** with a technique whereby it is possible to *greatly change the characteristics of the turbo codes, or to improve weight distribution of said codes* {See **Yamaguchi et al.**, Excerpt translation : page 1 last para first sentence.}

While the **Admitted prior art** and **Yamaguchi et al** substantially disclose the procedure for the claimed invention, **they fail to specifically describe** in detail the concept whereby random rearrangement of data is effected by exchanging data units at least between rows and columns.

However, such technique is well known in data processing systems, e.g., **de Almeida et al.**, in an analogous art, discloses an algorithm wherein such random rearrangement means is depicted. {See **de Almeida et al.**, Id., Example 1, Fig.1 and Table 1.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Admitted prior art** and **Yamaguchi et al** by including therein the technique as disclosed by **de Almeida et al.** because such modification would provide the procedure of **Admitted prior art** and **Yamaguchi et al** with a method whereby " *simple random-error-correcting codes can be used to correct clusters of*

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errors, instead of the more complex burst-error-correcting codes. “ {See **de Almeida et al. Id.**,

SUMMARY: para. 1 last sentence, and col. 1 penultimate para. }

2.4 Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants’ Admitted prior art** (hereinafter **Admitted prior art**) in view of **Karasawa et al.** (US Patent No. 5,204,981; Mar. 1, 1991) in further view of **de Almeida et al.** (Two-Dimensional Interleaving Using the Set Partitioning Technique; IEEE, Aug. 1994).

As per Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49, Admitted prior art substantially discloses the procedure for the claimed interleaving method comprising the steps of: arranging data to be transmitted in a matrix; and randomly rearranging at least either columns or rows of said data and outputting said rearranged data in time series. {See **Admitted prior art**, Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a random fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.} **Not specifically described** in detail in **Admitted prior art** is the step whereby rearranging by either columns or rows of data is performed in time series or sequentially.

However such approach is well known. For example, **Karasawa et al.**, in an analogous art, discloses algorithms wherein such techniques are described. {See **Karasawa et al.**, Id., Fig. 9 and Abstract: last line.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of the **Admitted prior art** by including therein a permutation method as taught by **Karasawa et al.**, because such modification would provide the procedure disclosed in the **Admitted prior art** with a technique whereby it is possible to design “*An interleaver 10 which stores a fixed amount of signal sequence output from the FEC coder 9 and outputs it in a time series different from that of the*

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input. That is, the interleaver 10 stores a fixed amount of data in a predetermined two-dimensional memory and provides the output, for example, in a column order if the input was applied in a row order.” {See Karasawa et al., col. 3 lines 5-et seq.}

While the Admitted prior art and Karasawa et al substantially disclose the procedure for the claimed invention, they fail to specifically describe in detail the concept whereby random rearrangement of data is effected by exchanging data units at least between rows and columns.

However, such technique is well known in data processing systems, e.g., de Almeida et al., in an analogous art, discloses an algorithm wherein such random rearrangement means is depicted. {See de Almeida et al., Id., Example 1, Fig.1 and Table 1.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of Admitted prior art and Karasawa et al by including therein the technique as disclosed by de Almeida et al. because such modification would provide the procedure of Admitted prior art and Karasawa et al with a method whereby " *simple random-error-correcting codes can be used to correct clusters of errors, instead of the more complex burst-error-correcting codes.* " {See de Almeida et al. Id., SUMMARY: para. 1 last sentence, and col. 1 penultimate para.}

2.5 Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable Karasawa et al. (US Patent No. 5,204,981; Mar. 1, 1991) in view of Yamaguchi et al. ("Turbo Code", a new coding system approaching theoretical Shannon limits, is born in France; NIKKEI ELECTRONICS, July 13, 1988) in further view of de Almeida et al. (Two-Dimensional Interleaving Using the Set Partitioning Technique; IEEE, Aug. 1994).

As per Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49, Karasawa substantially discloses the procedure for the claimed interleaving method comprising the steps of: arranging data to be transmitted in a matrix; and randomly rearranging at least either columns or rows of said data and outputting said rearranged data in time series. {See Karasawa ,

Fig. 9, Abstract: last line and col. 3 lines 5-et esq., in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a some fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.} **Not specifically described** in detail in **Karasawa** is the step whereby random rearranging by either columns or rows of data is effected.

However such approach is well known. For example, **Yamaguchi et al.**, in an analogous art, discloses algorithms wherein such techniques are described. {See **Yamaguchi et al.**, Id., Excerpt translation : page 1 first and second paras. last line.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Karasawa** by including therein a random permutation method as taught by **Yamaguchi et al.**, because such modification would provide the procedure disclosed in **Karasawa** with a technique whereby it is possible to *greatly change the characteristics of the turbo codes*, or *to improve weight distribution of said codes* {See **Yamaguchi et al.**, Excerpt translation: page 1 last para first sentence.}

While Karasawa and Yamaguchi et al substantially disclose the procedure for the claimed invention, **they fail to specifically describe** in detail the concept whereby random rearrangement of data is effected by exchanging data units at least between rows and columns.

However, such technique is well known in data processing systems, e.g., **de Almeida et al.**, in an analogous art, discloses an algorithm wherein such random rearrangement means is depicted. {See **de Almeida et al.**, Id., Example 1, Fig.1 and Table 1.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Karasawa and Yamaguchi et al** by

including therein the technique as disclosed by **de Almeida et al.** because such modification would provide the procedure of **Karasawa and Yamaguchi et al** with a method whereby "*simple random-error-correcting codes can be used to correct clusters of errors, instead of the more complex burst-error-correcting codes.*" {See **de Almeida et al. Id.**, SUMMARY: para. 1 last sentence, and col. 1 penultimate para.}

2.6 Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable **Karasawa et al.** (US Patent No. 5,204,981; Mar. 1, 1991) in view of **Azuma et al.** (US Patent No. 4,959,863; June 2, 1988) in further view of **de Almeida et al.** (Two-Dimensional Interleaving Using the Set Partitioning Technique; IEEE, Aug. 1994).

As per Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49, Karasawa substantially discloses the procedure for the claimed interleaving method comprising the steps of: arranging data to be transmitted in a matrix; and randomly rearranging at least either columns or rows of said data and outputting said rearranged data in time series. {See **Karasawa** , Fig. 9, Abstract: last line and col. 3 lines 5-et esq., in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a some fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.} **Not specifically described** in detail in **Karasawa** is the step whereby random or variable rearranging by either columns or rows of data is effected.

However such approach is well known. For example, **Azuma et al.**, in an analogous art, discloses algorithms wherein such techniques are described. {See **Azuma et al.**, Id., Abstract.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Karasawa** by including therein a mathematical method as taught by **Azuma et al.**, because such modification would provide the procedure disclosed in **Karasawa** with a technique whereby the "[The] decimated signal sequence (signal

vector) *Y.sup.i'* (*Z.sup.16*) is permuted by a multiplication by the permutation matrix *[T]* of 8.times.8. In this case, the row element of the permutation matrix is 0 or 1 (the sum being 1), and element of this matrix is 0 or 1 (the sum being 1). The permutation matrix is a fixed permutation if constant with time, and a variable permutation if variable. In the scramble processing, the rows of this matrix are permuted at random, and the number of combinations is usually $n!$ for an n .times. n matrix.” {See Azuma et al., col. 10 line 59-et seq.}

While Karasawa and Azuma et al substantially disclose the procedure for the claimed invention, they fail to specifically describe in detail the concept whereby random rearrangement of data is effected by exchanging data units at least between rows and columns.

However, such technique is well known in data processing systems, e.g., de Almeida et al., in an analogous art, discloses an algorithm wherein such random rearrangement means is depicted. {See de Almeida et al., Id., Example 1, Fig.1 and Table 1.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of Karasawa and Azuma et al by including therein the technique as disclosed by de Almeida et al. because such modification would provide the procedure of Karasawa and Azuma et al with a method whereby " *simple random-error-correcting codes can be used to correct clusters of errors, instead of the more complex burst-error-correcting codes.* " {See de Almeida et al. Id., SUMMARY: para. 1 last sentence, and col. 1 penultimate para.}

Drawings

3. The Drawings are objected to because Figures 22-24, referred to as conventional in the specification, have not been labeled as prior art. Appropriate correction to drawings as required by form PTO 948 shall be made in response to current Office action as per 37 CFR 1.85(a).

Specification

4. The disclosure is objected to because said disclosure recites: "row 14" on page 6 lines 9-12 which is not seen in Fig. 14.. Appropriate correction is required.

Claim Objections

5. Claims 31-42, 46 and intervening claims are objected to for including in passim "second storing unit," recitation that suggests the existence of a first storing unit. Appropriate correction is required.

Claim Rejections - 35 USC § 112 SECOND PARAGRAPH

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- 6.1. There is insufficient antecedent basis for "the error correcting code" in Claims 43, 49 and intervening claims.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

- 7.1 The prior art made of record and relied upon is considered to applicant's disclosure. The references are cited in Form PTO-892 for the Applicant's review and comments.

- 7.2 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 746-7238, (for After-Final communications),

(703) 746-7239, (for formal communications intended for entry),


(703) 746-7240 (for informal or draft communications, please label
"PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,
Arlington, VA, **Fourth Floor** (Receptionist).

Any inquiry concerning this communication or earlier communications from the
examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-
0755. The examiner can normally be reached on Monday to Friday from 8:30 AM to 5:00 PM.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's
supervisor, Albert Decady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding
should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Guy J. Lamarre, P.E. 

Patent Examiner

5/1/02


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